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Analog/RF circuit design techniques for nanometerscale IC technologies

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Abstract:

CMOS evolution introduces several problems in analog design. Gate-leakage mismatch exceeds conventional matching tolerances requiring active cancellation techniques or alternative architectures. One strategy to deal with the use of lower supply voltages is to operate critical parts at higher supply voltages, by exploiting combinations of thin- and thick-oxide transistors. Alternatively low voltage circuit techniques are successfully developed. In order to benefit from nanometer scale CMOS technology, more functionality is shifted to the digital domain, including parts of the RF circuits. At the same time, analog control for digital and digital control for analog emerges to deal with current and upcoming imperfections.

1. Introduction

In the past decade electronic systems have popped up everywhere in our society. They are very cheap in relation to their (added) functionality and sometimes even just become fashion items, like mobile phones and MP3 players. Mass production using Integrated Circuits is the key to low cost systems. Thanks to integration, board design becomes easier and with the right software, systems can be produced at low cost. Today systems are highly digitized, enabling this integration in CMOS technology.

The evolution in CMOS technology is motivated by decreasing price-per-performance for digital circuitry; its pace is determined by Moore's Law. To ensure sufficient lifetime for digital circuitry and to keep power consumption at an acceptable level, the dimension-shrink is accompanied by lowering of nominal supply voltages. While this evolution in CMOS technology is by definition very beneficial for digital, this is not so for analog circuits [1,2,3].

Contemporary IC's are mixed-signal systems consisting of a large digital core including amongst others a CPU or DSP and memory, often surrounded by several analog interface blocks such as I/O, D/A and A/D converters, RF front ends and more. From an integration point of view all these functions would ideally be integrated on a single die. In this case the analog electronics must be realized on the same die as the digital core and consequently must cope with the CMOS evolution dictated by the digital circuit.

In order to analyze the need from a circuit point of view we first look at the trends in systems and then at the trends in CMOS technology. It's the task of the circuit designer to bridge the widening analog gap between the system demands and the available CMOS technology.

2. Systems

The trend in system design is twofold. On one hand there is a trend to integrate more functionality in a single multi-purpose device; examples of this include PC's, palmtop computers or mobile telephones. These systems consist of a general purpose digital calculation core, with a reconfigurable user interface and with a limited amount of dedicated I/O functionality. Using these systems, a multitude of different task can be carried out. These tasks range from the bare functionality (e.g. making a phone call) to playing music, playing games, playing movies, playing… Functionality can easily be added by adding software. In this first class of systems software is run and signals are processed in the digital domain. The digital core of these systems is therefore preferably manufactured in advanced CMOS technology to get low *cost* per computation and at the same time low *power* per computation.

On the other hand there is the trend to make more distributed, invisible electronic systems that target at collecting or delivering data. In general these (for the user) invisible systems are used to control other systems and as such are highly optimized for one specific task, such as sensing the oil pressure in a car or RFID. These systems can be seen as sensors or I/O devices for a larger system. The core of this larger system usually is a programmable multi-purpose device: a system of the first kind. The sensory electronics contain dedicated sensors and communication hardware and little intelligence; they can be produced in a technology which is optimized for these functions which typically is not advanced CMOS because of cost reasons and the little need for a big digital core.

Analog in systems

Almost all systems need to interface with the real analog world. Since the signal processing mainly is done in the digital domain for efficiency reasons, the required AD converters and DA converters are moving to the edge of the system. At the same time, traditionally digital blocks such as I/O are becoming more and more analog due to either high-speed requirements or to high-voltage requirements. Just like for any analogish circuit, AD

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converter performance comes at the cost of area and power consumption. For this reasons it remains beneficial to put analog preprocessing circuits like amplifiers, filters and frequency translation circuits in front to the ADC to relax its performance demands.
Since the 70s researchers try to integrate these circuits in CMOS technology, which is primarily developed for digital circuits. The advantage of integrating analog with digital circuits is the resulting compact and low-cost single chip solution. During the eighties analog video baseband circuits were integrated in CMOS, covering the low MHZ frequency range. In the nineties also RF circuits for the low GHz range could be designed in CMOS because the speed of the technology became sufficient meanwhile. While companies were reluctant to put RF circuits in CMOS, universities continued research and developed new techniques. Today fully integrated RF transceivers, including digital baseband and MAC layers can be produced on one single CMOS die [4,5,6]. Maybe single chip CMOS transceivers are not the best performing or most cost effective solutions today, but thanks to a lot of research effort, the problems are solved bit by bit.

Analog challenge from a system point of view
The next challenge for the analog designers form a system point of view can be split into two directions. The first one is to use the technology advances, and move to higher frequencies, like 60GHz communications and radar. The second direction is to digitize the RF sections to achieve both higher programmability and higher flexibility for multiple standards RF. This trend is towards e.g. software radio [7,8].

3. Technology issues

In the past few decades of technology evolution, planar bulk CMOS was scaled to lower and lower dimensions, breaking foreseen limits to scaling all the time. However, there is a consensus that scaling of planar bulk CMOS will stop in the near future, around the 45nm node. In this section first some issues concerning more or less conventional CMOS scaled down to the 45nm node are addressed. In section 6, a number of items related to the successor of the planar bulk device are reviewed.

3.1 Output conductance effects

One of the major issues in analog design is transistor gain, and its linearity aspects. As shown in [3] these are improving with newer CMOS technologies provided the voltage headroom and the transistor length are not scaled down. This is illustrated in Figure 1: the gain and the IP3 do not change significantly with newer technologies at constant transistor length L and at constant voltage headroom. With lower voltage headroom the performance of transistors decreases.

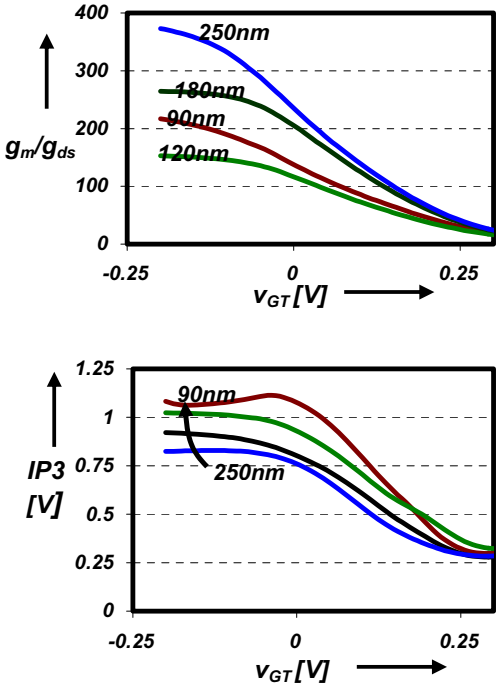


Figure 1: Various DC-properties of transistors as a function of the gate-overdrive voltage with V_{DS} =0.3V and L=1um for 4 technologies: (a) the gain, and (b) the output IP3

In ultra-deep sub-micron (UDSM) CMOS technologies, the transistor gain is lower-limited by requirements of the digital circuitry. For its robustness at least a voltage gain of about 10 is required using the minimum-length devices which also results in the relatively weak relation between output conductance and technology shown in Figure 1. However, scaling conventional planar bulk devices will stop because of the problems associated with getting sufficient (digital) gain below the 45nm technology node. A discussion of the foreseen solutions is presented in section 4.

3.2 Gate leakage effects

One of the relatively new effects in ultra-deep submicron CMOS is the significant gate-leakage. One of the first areas where this became eminent was in low-frequency applications such as PLL-loopfilters and hold-circuits with long time constants. In nowadays UDSM CMOS gate-leakage may be a serious problem for analog circuit design because:

- it poses a lower limits to the usable frequency range for integrator circuits; e.g. for filters and hold-circuits
- it introduces a strong relation between DC-current gain and transistor length, which effectively limits accuracy
- its mismatch introduces a new limit to achievable accuracy
- shotnoise is due to gate-current

All these effect can easily be estimated using the f_{gate} of a MOS transistor. This area-*in*dependent and fairly v_{DS}-independent parameter is for conventional MOS transistors [3]:

$$f_{gate} = \frac{g_{tunnel}}{2\pi C_{in}}$$
$$\cong 1.5 \cdot 10^{16} \cdot v_{GS}^2 \cdot e^{t_{ox}(v_{GS}-13.6)} \quad (NMOST)$$
$$\cong 0.5 \cdot 10^{16} \cdot v_{GS}^2 \cdot e^{t_{ox}(v_{GS}-13.6)} \quad (PMOST)$$
$$t_{ox}\ in\ [nm] \qquad v_{GS}\ in\ [V]$$

Figure 2 shows f_{gate}–bands for 4 technologies as derived from measurements. This figure shows that f_{gate} ranges from roughly 0.1Hz in 180nm technologies to about 1MHz in 65nm CMOS; for PMOS-transistors, f_{gate} is roughly a factor 3 lower. This f_{gate} can be used to easily estimate the impact of gate leakage on other relevant properties of MOS transistors.

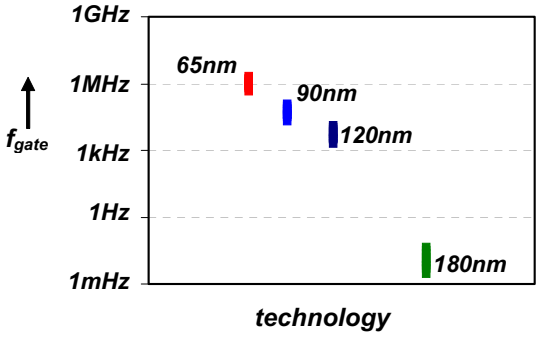


Figure 2: f_{gate} ranges for typical analog applications, for NMOS-transistors in different CMOS technologies. For PMOS-transistors f_{gate} is roughly a factor 3 lower.

The impact of gate-leakage on filters, integrators and hold circuits

The f_{gate} by definition gives the frequency below which the input impedance appears to be mainly resistive. For frequencies higher than f_{gate} the gate appears to be mainly capacitive. For filters this simply implies that a MOS-capacitance can be used as capacitance only for frequencies much higher than the f_{gate}. For lower frequencies a (loop-)filter using MOS capacitances effectively is a (non-linear) resistive divider. This leaky behavior of gates also severely limits applications in switched-current circuits and sample-and-hold circuits. The droop-rate of MOS-capacitances is as a good approximation given by:

$$\frac{dv_C}{dt} \approx -\gamma_{dvdt} \cdot f_{gate} \quad \left[\frac{V}{s}\right] \qquad with \quad \gamma_{dvdt} \approx 1V$$

which relation implies that when accepting a droop of ΔV, the maximum (hold-)time is

$$\Delta t \approx \frac{\Delta V}{\gamma_{dvdt} \cdot f_{gate}} \quad [s]$$

Allowing, e.g., 1mV drop on a sampled-and-held value, the maximum usable hold-time is in the ms-range in 180nm technologies, which is usually sufficient. However the maximum hold time decreases rapidly with newer technologies, down to a typical value in the low nano-second range for standard 65nm technologies. To get an acceptable hold-time in 65nm CMOS, either thick oxide transistors or inter-metal capacitances must be used; similar conclusions hold for PLL loop filters.

Leaky gates result in DC-input current, which sets a lower bound on the current gain of a MOS transistor; as a rough estimation this DC gain is:

$$\frac{i_D}{i_{GS}} \approx \frac{1}{L^2} \cdot \frac{\mu \cdot (v_{GT} - V_T)^2}{2 \cdot \beta_{igs} \cdot f_{gate}} \qquad with \quad \beta_{igs} \approx 1V$$

For a typical 65nm CMOS generation and at low effective gate-overdrive voltages, the current gain is about unity for $L \approx 30\mu m$.

The impact of gate-leakage on matching

Gate leakage is caused by quantum-mechanical tunnelling and depends on the layer-thickness and the field-strength. It therefore exhibits spread that can limit the achievable level of performance of analog circuits. Because spread and mismatch are DC effects, they do not (from a fundamental point of view) require any additional power. However, the typically way to minimization is spending area [9,10] which in turn increases power consumption at a given speed, because larger capacitances have to be charged [11].

Gate-leakage mismatch is an extra mismatch source [3] with an area-dependency *different* from that of conventional matching [9,10,12]. Mismatch of gate leakage current is proportional to the gate current level with in 65nm CMOS a proportionality constant $X_{IGS} \approx 0.03/\sqrt{Area}$, where *Area* is the transistor's gate area in square-micron. The total relative mismatch of a transistor's drain current is roughly given by the following relation; current factor mismatch of the transistors is neglected, which is allowed for practical values of v_{GT} [10].

$$\frac{\sigma_{id}^2}{i_D^2} = \frac{\sigma_{id,conventional}^2}{i_D^2} + \frac{\sigma_{id,gateleakage}^2}{i_D^2}$$
$$= \left(\frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{i_D}\right)^2 + \left(\frac{X_{IGS}}{\sqrt{WL}} \cdot \frac{i_G}{i_D}\right)^2$$

The first term is the conventional mismatch due to mismatch in threshold voltage, with A_{VT} the matching coefficient. This A_{VT} is a technology-related factor that is roughly proportional to the gate-oxide thickness, saturating in UDSM technologies around 2-3mVμm [12]. The second term is the gate current mismatch. The impact of gate-leakage mismatch on the overall mismatch is best illustrated using the square-law relation which relation is sufficient for rough estimation purposes. It follows that:

$$\frac{\sigma^2_{ID}}{i^2_D} = \left(\frac{A_{VT}}{\sqrt{WL}} \cdot \frac{g_m}{i_D} \right)^2 + \left(\frac{\zeta \cdot f_{gate} \cdot L^2}{\sqrt{WL}} \right)^2$$

In this relation ζ is a constant that is independent of area and (almost) independent of technology. It follows directly that high values of f_{gate} result in a large impact of gate-leakage related mismatch. The previous relation also shows that by *linearly* scaling of transistors (increasing the width and the length proportionally), with constant power consumption, the classical mismatch term decreases while at the same time the gate-leakage term increases. This yields a maximum usable area and a lower limit on attainable mismatch. With width-scaling and a proportional power-scaling there is no minimum in the reachable mismatch figure. It's also clear that the f_{gate} has a significant impact on the minimum attainable mismatch figure: for maximum matching therefore low-leakage devices should be used.

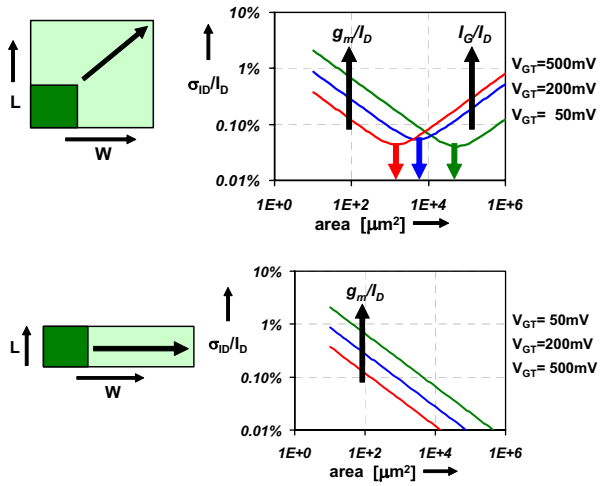


Figure 3: The spread of an MOS transistor in 65nm CMOS with a) linear scaling of *W* and *L* at constant power consumption b) W-scaling, and proportional powerscaling

3.2.1 The impact of gate-leakage on noise

Just as any current across a junction, gate leakage exhibits shot-noise with current density $S_{IG} = 2q \cdot I_G$. As such, it is equivalent to base-currents in bipolar transistors. This shot noise comes on top of the induced gate noise [13,14]. Noise in the gate current therefore limits noise performance in analog circuits in UDSM CMOS [15].

4. Future CMOS transistors

In the past few decades, the transistors in mainstream CMOS technology were planar bulk devices. Scaling of these planar bulk devices is expected to end around the 45nm technology node [16,17]. The most likely successors are fully depleted (FD) thin-body transistors [17,18]. These FD thin-body transistors have a number of advantages over conventional UDSM transistors:

- the suppression of short channel effects is relatively good
- the output conductance can be relatively low
- the sub-threshold slope of these devices is near ideal: about 60mV/decade
- the junctions are small because of the thin-body enclosed by oxide

The fully depleted transistors are basically thin-film SOI transistors that come in many flavours. Figure 4b shows the type that resembles the planar bulk device in Figure 4a the most. The double-gate variant that probably is the successor or the planar bulk devices is the FinFET [17,19,20,21,22] shown in Figure 4c and 4d. The naming of the FinFET originates from its appearance, see also Figure 4d for a simplified view; the device resembles a silicon fin on top of a SiO_2 layer, with the gate draped over it to effectively form a gate on (usually only) both sides of the fin.

As conduction takes place on the two sides of the fin, the *W* of the FinFET is twice the height of a fin (this fin-height is therefore denoted as *W/2* in Figure 4d). The fin–width is small in order to get fully depleted devices with decent properties: as a rule of thumb the fin-width is smaller than *L/4* which amounts to only 10nm wide fins for 40nm long transistors [23]. Taking into account the current shape of the fins [24], the *W* of FinFETs is heavily discretized at about $W \cong 2N \cdot L_{min}$ with N=1,2,3,… and with L_{min} the minimum transistor length.

There are many differences between the conventional planar bulk MOS transistors and the (FD SOI) FinFETs. Below a short summary is given, focussing on some analog aspects not listed in the previous list.

- The body of the FinFET will be almost undoped, while the threshold voltage will be determined by the workfunction between the silicon and the metal gate [25]. As a result both gate depletion and threshold voltage spread due to dopant number fluctuations in the body are essentially absent.
- Vt-spread will be determined by the spread in the fin-width [25] and by the spread in the workfunction. There's not yet good data of expected mismatch and area-scaling relations.
- Conduction takes place on the sidewalls of the fin, which are formed by etching: this surface is rough which probably gives rise to excess flicker noise.
- The gate-leakage of FinFETs is reduced by about one order of magnitude compared to that in planar devices because of reduced fields and quantum confinement effects [26].
- The mobility and hence the transistor's current factor is orientation dependent in FinFETs because of the conduction on the sidewalls of the fin: the crystal orientation can be anything ranging from (1 0 0) to (1 1 0) [21,27] which significantly affects carrier mobility. This orientation dependency is expected to give no problems in analog circuit design as it is good practice to layout matching sensitive transistors in the same orientation.

- Heat transfer of transistors is lower in SOI transistors compared to bulk devices: the thermal conductivity of SiO_2 is about two orders of magnitude lower than that of Si. For typical analog applications of transistors, with a relatively low gate-source overdrive voltage and drain-source voltage, this may result in heating of transistors. Heating results in shifted transistor parameters that may result in mismatch or thermal hysteresis effects [28, 29]. For accurate analog models, the temperature may have to be included as a state-variable.

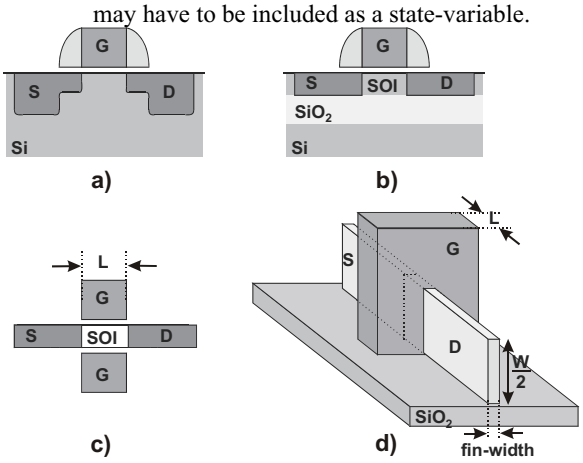


Figure 4 Upcoming evolution in CMOS transistor structure a) the conventional planar bulk device b) the single-gate thin-body SOI transistor c) top-view of a FinFET d) side-top view of a FinFET

All together, the FinFETs have a number of parameters that are better than those of conventional devices: output conductance, gate-leakage and junction capacitances are lower. A number of new effects are introduced; most notably new mismatch effects, heating effects and flicker noise which introduce many unknowns in circuit design. With the current design aspects of UDSM CMOS technologies [3] this gives many new research opportunities.

5. Circuit design challenges and opportunities

From a system point of view analog/RF moves to either higher speeds or higher flexibility, enabling software signal processing. From a technology point of view the speed of the transistors increases, digital properties improve, while at the same time the analog properties get worse. With this in mind the role of analog circuits for the future can be predicted. In order to do so, we propose to classify 4 types of electronic circuits:

1. Pure digital circuits
2. Analog circuits for digital
3. Digital circuits for analog
4. Pure analog circuits

1. Pure digital circuits

Pure digital circuits will continue to grow in complexity. Driven by Moore's law the number of gates will grow exponentially, and cost effective ICs will exploit the high gate count. Such complex ICs are hard to oversee and this is one of the reasons why digital ICs will contain multiple cores (or tiles) of processors, memory, and dedicated digital hardware. The cores can operate in parallel [30], at locally high speeds and relatively slow networking over the "large distances". The pure digital design work is highly automated, and higher order description languages like VHDL are common practice today. Digital designers don't have to worry much about gate level design anymore; however the challenge is to oversee such a complex system. To develop a complex IC in a modern technology is very expensive and therefore it is beneficial to use the same IC (hardware) in different applications by programming its functionality in software. One of the great challenges is to program such a system in an effective way since parallel processing is badly supported by todays programming languages.

Digital ways to increase the robustness of essentially digital systems include parity checks and ECC (error checking and correcting) [31] which are mainly found in memories and in communication channels.

2. Analog circuits for digital

Pure digital ICs contain a few basic true analog functions like power-on-reset and a PLL for internal high speed low jitter clock generation which obviously cope with classical analog implementation problems. However also the "pure digital" circuits face analog problems. One of the first problems encountered was signal integrity [32]: digital switching itself creates bounce on supplies and substrate nodes in such a way that gate speed drops significantly and even functional errors result. Proper on-chip decoupling can solve these problems at the cost of area [32].

The power consumption of digital ICs strongly depends on the supply voltage and the clock frequency. To minimize power consumption, adaptive supply voltages and clocks can be used. To implement this, DC-DC converters can be used in control systems where both the clock frequency and the supply are lowered in such a way that the calculation is done just in time. This adaptive supply can yield significant power savings in practical ICs [33, 34].

Another application of emerging analog control for digital circuits is the inclusion of many analog circuits as sensors in large digital ICs. Doing so, immunity towards process variation and temperature margin does not need to be taken into account in the design, which may save a considerable amount of overhead and power consumption. Examples include measuring the local supply voltage [35], the local temperature [36], jitter etc and adapting to them. Another application of sensory electronics in combination with actuators is the cancellation of unwanted disturbances [37].

Another issue related to power supply of digital ICs is the compatibility of new products with old ones. The

internal supply voltage of ICs has been dropping the past decade from 5V down to 1 V today. However lagging behind, the PCB board designs still use higher voltage swings and supplies as standards. For this reason the modern digital ICs should sometimes still look, from the outside, as if they operate on a higher supply voltage than used internally. This is especially the case for commodity products like microcontrollers. For this reason fully integrated supply voltage regulators [38,39] and high voltage IO buffers [40] have been developed in modern CMOS technologies. These circuits are designed at a higher than nominal supply voltage, but by carefully stacking devices the circuits can withstand the high voltages.

The on-chip communication is getting more attention, as (global) interconnects are rapidly becoming a speed, power and reliability bottleneck for digital systems [41]. Technological advances such as copper interconnects and low-k dielectrics are not sufficient to let the interconnect bandwidth keep up with the advances in transistor speeds.

From a circuit-design perspective, a general solution is the use of repeaters, which is expensive in term of area and power. Another proposed solution [42] uses low-swing signaling over differential 10mm aluminum interconnects. In [43], it is proposed to use 16µm-wide differential wires (20mm long) and exploit the LC regime (transmission line behavior) of these wires.

In [44], it is shown that pulse-width pre-emphasis in combination with resistive termination can increase the data-rate to 3Gb/s/ch, using 10mm-long, 0.4µm-wide differential interconnects. Without the proposed techniques, these interconnects can achieve only 0.55Gb/s/ch. So by using analog equalizers which still comply with pure digital swing, a factor 6 in speed increase can be achieved over large distances.

3. Digital circuits for analog

Analog CMOS circuits typically reside on an IC that has digital signal processing circuits. Since digital circuits have become very compact, analog circuits can nowadays receive help from digital circuits: the analog circuits can be calibrated and can be corrected for the non ideal behaviour. This calibration can be online, while normal signals are processed, or offline in a special calibration mode. This correction in turn can be done in the analog domain (where typically a DA converter injects a static signal in the analog circuit) or in the digital domain (where an error can be subtracted). Below some examples of calibrated circuits are given.

This trend of calibrating is clearly observable in AD converters. In pipeline ADC's amplifier non-linearities are a major concern and in [45] background calibration was implemented to correct for these sources of impairment. This allows the use of simple power-efficient open-loop residue amplifiers, which are more compatible with modern CMOS technologies.

ADCs can even be calibrated on line in background, with a calibrated auxiliary ADC. In [46] a pipelined analog-to-digital converter (ADC) is calibrated in background using an algorithmic ADC, which is itself calibrated in foreground. The calibration overcomes the circuit non-idealities caused by capacitor mismatch and finite operational amplifier (opamp) gain both in the pipelined ADC and the algorithmic ADC.

Digital calibration is also used in RF circuits: for example in [47] calibration techniques are presented that suppress the carrier leakage and enable the direct-upconversion architecture to meet WCDMA specifications.

Another example is found in [6] where a closed-loop RF calibration is used in a fully integrated transceiver, including digital MAC layers. An RF loop-back path is used from the output of the transmit mixer to the input of the receive mixer. During calibration, a known digital sequence is transmitted and looped back to the receiver and the received digital signal is used to correct for analog and RF non-idealities such as DC offset, I/Q mismatch, and RF carrier leak. This way matching requirements are relaxed and area and power can be saved.

If we observe this trend, then we can foresee analog circuits, with many calibration points. Smart algorithms can locate the error sources in the digital domain and correct for it. These way at least static errors (gain, mismatch, and even linearity) can be compensated. However, noise cannot be compensated for in the digital domain due to its wide band nature: it remains an analog problem. On the system level, however, detection algorithms can be improved so that less signal-to-noise is needed for the required bit error rate. For example in RF circuits, inductors are used today to improve the signal to noise ratio. If we realize that an inductor of a few nH - which is necessary for the low GHz range - occupies the same die area as a simple baseband processor in 65nm technology, it is clear that smart digital detection techniques can help to overcome noise problems as well.

4. Pure analog circuits

Analog once was the field in which the main chunk of signal processing was done. Since a few decades a continuous shift towards digital signal processing with some analog processing (or conditioning) of the inputs and outputs of the digital core is apparent. However, still analog circuits are required to get meaningful data into and out of the digital core in an area-efficient and power-efficient way. Although the area where pure analog is applied will inevitably shrink to a (non-zero) minimum, the requirements on analog circuits will continue to increase while the CMOS implementation environment gets worse and worse.

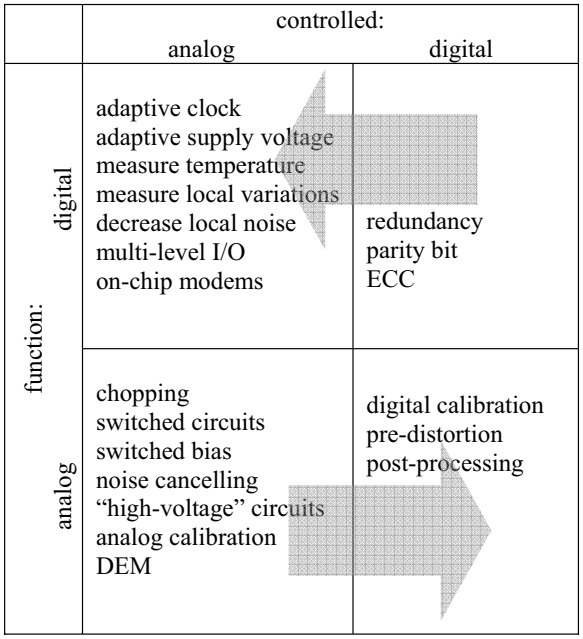
One fundamental problem for analog CMOS circuits is the lowering supply voltage. This problem can be tackled in 2 ways. Design analog circuits that operate at a low voltage or design analog circuits that can withstand higher than nominal supply voltages.

The first approach was popular during the past 15 years where the supply dropped from 5V down to 1.2 V today. Many new circuit techniques have been developed recently, for example the switched opamp technique [48] where switches in switched capacitor are moved from the signal path to the supply path, where they need less gate drive. Recently a similar approach has been demonstrated for Gilbert type of mixers [49]

Despite all the research effort, today the bare minimum supply for an analog circuit seems to be $V_{GS}+V_{DSSAT}+v_{swing}$, where v_{swing} is the signal swing. If still enough SNR is needed then the noise has to be lowered. This can simply be done via impedance level scaling, and the result is that 10dB less noise will result in 10 times more power consumption (for the same supply voltage, SINAD, bandwidth, etc).
Thermal noise can even be cancelled [50] but also at the cost of power dissipation. 1/f noise is a major concern as well since the corner frequency, where thermal noise dominates the 1/f noise seems to be proportional to f_t in a given technology. So since f_t is usually chosen high, to benefit from the bandwidth, 1/f noise will be large as well. Chopping and double correlated sampling can remove 1/f noise for low frequency application. Switched bias technique can reduce the intrinsic 1/f noise of transistors [51]
The second approach is to design circuits that can withstand higher than nominal supply voltages. This is usually done via stacking of transistors while taking care that each transistor does not breakdown, including during transients and startup.
These circuits at higher supply were first found in interfacing drivers [40] and later in (RF) PAs [52,53], but nowadays also normal "internal" analog circuits need to use these techniques to get performance at todays 1V supply voltage. This can be done, but careful simulation has to be done by the designers, because moderate breakdown effects are hard to see during production test and may show up during the lifetime of the IC.

Analog circuits will operate at higher frequencies as well. At high frequencies it's beneficial to use inductors for high Q circuits, like oscillators and tuned amplifiers Inductor quality factors (Q) increase with frequency and at frequencies beyond say 40GHz Q factors of integrated spiral inductors are higher than the Q factors of the resonating capacitors. Realizing this, the designer does not have to take care for max Q of inductors, and also since that the values of inductances are small for high frequencies, the inductors can be laid out in a very compact way: for example in a compact U shape instead of a circle [54]. So for very high frequencies inductors can be used at many nodes in a circuit.

Wrap up
In the past decades, much functionality shifted from the (traditional) analog domain to the digital domain because of (area and power) efficiency reasons. Apart from this shift, there is also a clear trend towards mixing analog and digital. In the near future high-performance digital blocks include analog sensory and control systems, while analog circuits tend to include more and more digital compensation and control.



In the limiting case, every digital subblock has its own analog control block to eliminate e.g. interference and the effects of spread in components and operating conditions. At the same time every analog subblock (down to single transistors) comes with its own digital control to compensate for things like spread and low-frequency noise.

6. Conclusions

The evolution of CMOS technology will continue for many years to come, which is benificial for digital circuits but which is not so for analog. An extensive discussion of relatively new non-ideal effects such as gate-leakage and output conductance is given in this paper, as is a discussion of the probably successor of the conventional MOS transistor.
On system level, there has been a longlasting trend towards shifting as much functionality from the purely analog domain to the purely digital domain. From a high level of abstraction this trend will continue, but at closer look the purely analog and digital blocks will disappear: the strive towards more circuit performance out of less perfect transistors yields a clear trend towards analog control for digital and towards digital control for analog. In both ways, analog design knowledge becomes crucial for modern ICs, even if they are "purely" digital.

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